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Drift compensation system and method in a clock device of an electronic circuit

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DRIFT COMPENSATION SYSTEM AND METHOD IN A CLOCK DEVICE OF AN ELECTRONIC CIRCUIT

Technical field

The present invention relates to systems used to adjust the phase shift between the sampling clock and the data companion clock of an electronic chip adapted to receive data and in particular relates to a drift compensating system and method in a clock device of an electronic circuit.

Background

High speed electronic circuits such as electronic chips widely used today especially in the telecommunication systems are implementing electric interfaces consisting of a data and/or control high speed bus synchronized to one or more companion

clocks provided at the interface according to various standards.

To properly process data or control signals, it is necessary for an electronic component receiving these signals as inputs to sample them appropriately at their input point. This is generally achieved using a training sequence during which the emitter component delivers a number of known training patterns on data/control signals while a receiver component controls and tunes its input sampling circuitry to properly recognize these patterns prior to switch to the operational mode.

Another technique to ensure optimum data sampling without requiring any data training sequence is illustrated in Fig. 1. A variety of implementations can be found depending on component manufacturer technology as well as low level design options or requirements. One implementation example is described in Xilin application note XAPP268.

In the implementation of Fig. 1, the data are received as parallel inputs by input receivers 10 and transmitted to the input flip-flops 12 which are clocked by the sampling clock signals received on inputs 14 which are provided by a clock phase alignment circuit.

The clock phase alignment circuit 16 is built around a clock management circuit 18 which has the property of acting like a phase locked loop circuit and provides one (or more) clock signal frequency locked to an input reference clock and which phase is controlled with respect to the input reference clock. The latter is provided by the receiver 19 on input 20 which is (are) used as sampling clock for the data module as mentioned above. For this, the input clock drives an input flip-flop 21 (identical to data flip-flops 12) which is clocked by the output 22 and provides a sampled clock to control logic 24 which is typically a state machine. Control logic 24 monitors

the sampled clock and permanently controls the clock management phase shift.

On startup (i.e. After the module reset), the phase shift of the clock management circuit 18 is set to a known predetermined value. The control logic 24 then examines the sampled clock output and evaluates it against a theoretical result (i.e., a bit to 1 or to 0) that should be obtained when sampled properly. The control logic 24 then alters the phase shift by one step or a small number of steps by sending either a phase advance or a phase delay to the clock management circuit 18. The alter/evalutation operations are repeated until as many steps as necessary are scanned to determine a phase step validity window for which both input flip-flop setup and hold time are met to ensure a correct sampling. Once the window is determined, the control logic 24 asserts its "aligned" indicator 26 and the module can turn to the operational mode. Assuming an acceptable skew between the input data and the input clock and considering the close matching between devices in the same piece of silicon, the resulting alignment if suitable for the input clock signal is also suitable for data going across identical electronic structure.

In summary, the technique illustrated in Fig. 1 takes advantage of a clock signal to be a training sequence by nature and avoids to use a specific data sequence. It ensures a clocking circuitry to match input flip-flop setup and hold time for proper input data sampling. Unfortunately, this system runs only once at startup time and then freezes the clock circuitry unless the whole system is started again. Furthermore, silicon timing characteristics may vary in time depending on environment conditions (temperature, power, supply voltage ...) resulting in a drift which cannot ensure an optimum sampling.

Summary of the invention

Accordingly, the main object of the invention is to provide a system and to achieve a method enabling a clock circuit to be always in operational mode without requiring to reset the module in order to cancel a clock phase shift.

Another object of the invention is to provide a system and to achieve a method enabling any phase drift due to a change in silicon timing characteristics to be canceled without requiring to reset the module.

The invention relates therefore to a drift compensation system comprising a first clock phase alignment circuit adapted for providing an output clock signal which is frequency locked to an input reference clock signal, a second clock phase alignment circuit identical to the first clock phase alignment circuit but wherein the reference clock signal is the output clock signal provided by first clock phase alignment circuit, first deviation means at the output of the first clock phase alignment circuit for providing a first deviation between its current clock phase and its initial clock phase, second deviation means at the output of the second clock phase alignment circuit for providing a second deviation between its current clock phase and its initial clock phase, and a phase control logic adapted for providing first phase shift signals as inputs to the first clock phase alignment circuit in order to cancel the phase shift between the output clock signal and the reference clock signal in response to the difference between the first and the second deviations.

According to a second aspect, the invention relates to a drift compensation method for canceling the phase drift in a system as defined above comprising the steps consisting in aligning, at defined times, the clock phase in the second clock phase alignment circuit by frequency locking the output clock signal

to the input reference signal, determining the deviation for each of the first and second clock phase alignment circuits which is the difference between the number of current steps needed for the alignment of the circuit and the number of steps needed for the initial alignment, checking whether the second deviation needed for the second clock phase alignment circuit is different from the first deviation needed for the first clock phase alignment circuit, and if the second deviation is different from the first deviation, shifting by one step the phase of the first clock phase alignment circuit.

Brief description of the drawings

The above and other objects, features and advantages of the invention will be better understood by reading the following more particular description of the invention in conjunction with the accompanying drawings wherein :

- Fig. 1 is a block-diagram representing a prior art system currently used to cancel the clock phase shift in the clock circuitry of an electronic circuit ;
- Fig. 2 is a block-diagram representing a clock phase alignment circuit this has been improved to be incorporated in a drift compensation system according to the invention ;
- Fig. 3 is a block-diagram representing a preferred embodiment of the drift compensation system according to the invention ; and
- Fig. 4 is a flow chart of the drift compensation method according to the invention.

Detailed description of the invention

The prior art clock phase alignment circuit 16 illustrated in Fig. 1 has to be improved in order to be incorporated into the drift compensation system according to the invention by addition of some features illustrated in Fig. 2. These features are an additional output carrying information

regarding the number of phase steps the clock management circuit 18 is being run, additional inputs (tune up, tune down) requesting the control logic to advance or to delay the clock management circuit phase by one step (or a small fixed number of steps) and an additional output (time done) provided in response to "tune up" and "tune down" indicating that the requested operation has been completed. Advancing or delaying the clock management circuit phase by one step or a small fixed number of steps allows to smooth sampling clock phase variations without the need of additionnal circuitry: it acts as an buid-in integrator.

As illustrated in Fig. 3, two clock phase alignment circuits like the clock phase alignment circuit 16 of Fig. 1 are used in the drift compensation system according to the invention. The first clock phase alignment circuit 30 is driven by the input clock used as a reference clock. As already explained, on startup, the phase shift of the circuit is set to a known, predetermined value and after a processing time, it asserts its "aligned" output 32 meaning that the module is turned in the operational mode and provides operational sampling clock signals on the output 34. At this time, a sampling clock signal is taken from clock phase alignment circuit 30 and fed back by line 36 as input reference clock for a second clock phase alignment circuit 38. This allows to operate circuit 38 at exactly the same frequency as circuit 30 while avoiding additional load to the input clock circuitry.

At the same time that "aligned" line is asserted, the initial number of steps used to cancel the phase shift in clock phase alignment 30 is stored in a first register 40. Likewise, when the output line "aligned" 42 of clock phase alignment circuit 38 is asserted, the initial number of steps used to cancel the phase shift in this circuit is stored in a second register 44. Then, at each subsequent phase alignment operation, the number of steps which have been necessary to cancel the phase shift

are subtracted in subtractor 46 for clock phase alignment circuit 38 in order to know the deviation value for each circuit. Then, the phase control logic 50 which is typically a state machine performs a comparison between deviations provided by the first and the second clock phase alignment circuitry 30 and 38 in order to forward either a tune up signal or a tune down signal on lines 52 to the first clock phase alignment circuit 30 in order to control this one in the operation of canceling the phase shift. Note that the phase control logic 50 provides also a reset signal on line 54 to the clock phase alignment circuit 38, and the reset releasing signal on the same line to launch the phase shift operation by the clock phase alignment circuit 38.

Now, the method of drift compensation is described in reference to Fig. 4. The first step (step 60) consists in aligning the first clock phase alignment circuit 30, on startup, when the circuit has been reset released. It runs an alignment sequence while the phase control logic holds clock phase alignment 38 on reset state. When the alignment is done, clock phase alignment circuit 30 asserts its "aligned" output line 32.

At this point, the number of phase steps of phase clock alignment circuit 30 is frozen and the phase control logic 50 takes necessary actions to store its value as initial number of phase steps into register 40 (step 62). Phase clock alignment circuit 30 being aligned, the sampling clock on output line 34 can be used as operational sampling clock for data modules. Then, phase control logic 50 releases clock phase alignment circuit 38 and this one runs its own phase alignment sequence (step 64). When completed, "aligned" indicator on output line 42 is asserted, and the number of initial phase steps for clock phase alignment circuit is stored into register 44 (step 66).

After this initial alignment procedure, the electronic component is operational but phase alignment procedures are achieved from time to time or on a periodic basis and a number of phase steps necessary for the alignment different from the initial number of steps may be found. It is why the next step consists in evaluating the first deviation provided by subtractor 46 at the output of clock phase alignment circuit 30 and the second deviation provided by subtractor 38 at the output of clock phase alignment circuit 38 (step 68) and to compare them in phase control logic 50 (step 70). It must be noted that the two deviations are equal to zero at the initial pass for the two clock phase alignment circuits.

Assuming that there is a drift in silicon characteristics and that the deviation procedure for clock phase alignment circuit 38 has been run at least one time, the second deviation (for clock phase alignment circuit 38) is no longer zero. This deviation represents the shift in phase steps (that is a known fraction of a clock period) between the current optimum alignment and the initial alignment for clock phase alignment circuit 38. Therefore, there is a chance that the second deviation be different from the first deviation. If it is checked that the second deviation is greater than the first deviation (step 72), the clock phase alignment circuit 30 is phase shifted one step up (step 74) and the "tune done" signal is sent to phase control logic 50 on line 33 (step 76). If it is checked that the second deviation is less than the first deviation (step 78), the clock phase alignment circuit 30 is phase shifted one step down (step 80) and the "tune done" signal on line 33 is activated (step 82). Note that, since first and second clock phase alignment circuits 30 and 38 are operating at the same frequency, it makes sense to adjust the first clock phase alignment circuit 30 phase shift so that the difference between targeted new alignment with respect to the initial alignment becomes equal to the deviation of the second clock phase alignment circuit 38. This is achieved by tuning

the first circuit 30 in the appropriate direction using the tune lines 52.

In both cases (the first and the second deviations are different) and after the activation of the "tune done" signal, or if the two deviations are equal (step 83), an optional time delay is set by the phase control logic to start again the deviation procedure (step 84). Such a delay can be variable or defined on a periodical basis. When this defined delay is passed, a new alignment of the clock phase alignment circuit 38 is achieved (step 86) before the process loops back to the step of evaluating the first and the second deviations.

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CLAIMS

1. Drift compensation system comprising :

a first clock phase alignment circuit (30) adapted for providing an output clock signal which is frequency locked to an input reference clock signal,

a second clock phase alignment circuit (38) identical to said first clock phase alignment circuit but wherein the reference clock signal is said output clock signal provided by first clock phase alignment circuit,

first deviation means (40, 46) at the output of said first clock phase alignment circuit for providing a first deviation between its current clock phase and its initial clock phase,

second deviation means (44, 48) at the output of said second clock phase alignment circuit for providing a second deviation between its current clock phase and its initial clock phase, and

a phase control logic (50) adapted for providing first phase shift signals (52) as inputs to said first clock phase alignment circuit in order to cancel the phase shift between said output clock signal and said reference clock signal in response to the difference between said first and said second deviations.

2. Drift compensation system according to claim 1, wherein each one of said first and second phase alignment circuits (30, 38) comprises a clock management circuit (18) adapted for providing said output clock signal which is frequency locked to said input reference clock signal, and a control logic (24) which provides second phase shift signals in response to said output clock signal, each of said second phase shift signals being used as an input step by said clock management circuit to reduce to zero said phase shift step by step.

3. Drift compensation system according to claim 2, wherein said first or second deviation means include a register (40 or 44) for storing the initial number of steps used at the startup of the associated clock phase alignment circuit (30 or 38) for reducing said phase shift to zero and a subtractor (46 or 48) for subtracting said initial number of steps from the current number of steps necessary to reduce said phase shift to zero at any time after said startup in order to obtain respectively said first or second deviation.

4. Drift compensation circuit according to claim 3, wherein each of said first phase shift signals provided by said phase control logic is used as an input step by said first clock phase alignment circuit to reduce to zero said phase shift between said output clock signal and said reference signal.

5. Drift compensation method for canceling the phase drift in system according to any one of claims 1 to 4, comprising the steps consisting in :

- aligning, at defined times, the clock phase in said second clock phase alignment circuit (38) by frequency locking the output clock signal to the input reference signal,
- determining the deviation for each of said first and second clock phase alignment circuits (30, 38) which is the difference between the number of current steps needed for the alignment of said circuit and the number of steps needed for the initial alignment,
- checking whether the second deviation needed for said second clock phase alignment circuit (38) is different from the first deviation needed for said first clock phase alignment circuit, and
- if said second deviation is different from said first deviation, shifting by one step the phase of said first clock phase alignment circuit.

6. Drift compensation method according to claim 5, wherein said step of shifting consists in shifting one step up if said second deviation is greater than said first deviation or shifting one step down if said second deviation is less than said first deviation.

7. Drift compensation method according to claim 5 or 6, further comprising a previous step which consists in aligning on startup said first clock phase alignment circuit (30) and storing the number of phase shifts as an initial number of steps for said first clock phase alignment circuit.

8. Drift compensation method according to claim 7, wherein an aligned signal (32) is provided by said first clock phase alignment circuit (30) to said phase control logic (50) when said circuit has been aligned.

9. Drift compensation method according to claim 8, wherein said first clock phase alignment circuit (30) provides a sampling clock when said circuit has been aligned, said sampling clock being used as a clock for data modules.

10. Drift compensation method according to claim 9, wherein said second clock phase alignment circuit (38) is enabled to be aligned when said aligned signal (32) is provided by said first clock phase alignment circuit (30), the number of phase shifts needed for such an alignment being stored as an initial number of steps for said second clock phase alignment circuit.

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DRIFT COMPENSATION SYSTEM AND METHOD IN A CLOCK DEVICE OF AN ELECTRONIC CIRCUIT

Abstract

Drift compensation system comprising a first clock phase alignment circuit (30) adapted for providing an output clock signal which is frequency locked to an input reference clock signal, a second clock phase alignment circuit (38) identical to the first clock phase alignment circuit but wherein the reference clock signal is the output clock signal provided by the first clock phase alignment circuit, first deviation means (40, 46) at the output of the first clock phase alignment circuit for providing a first deviation between its current clock phase and its initial clock phase, second deviation means (44, 48) at the output of the second clock phase alignment circuit for providing a second deviation between its current clock phase and its initial clock phase, and a phase control logic (50) adapted for providing first phase shift signals (52) as inputs to the first clock phase alignment circuit in order to cancel the phase shift between the output clock signal and the reference clock signal in response to the difference between the first and the second deviations.

FIG. 3

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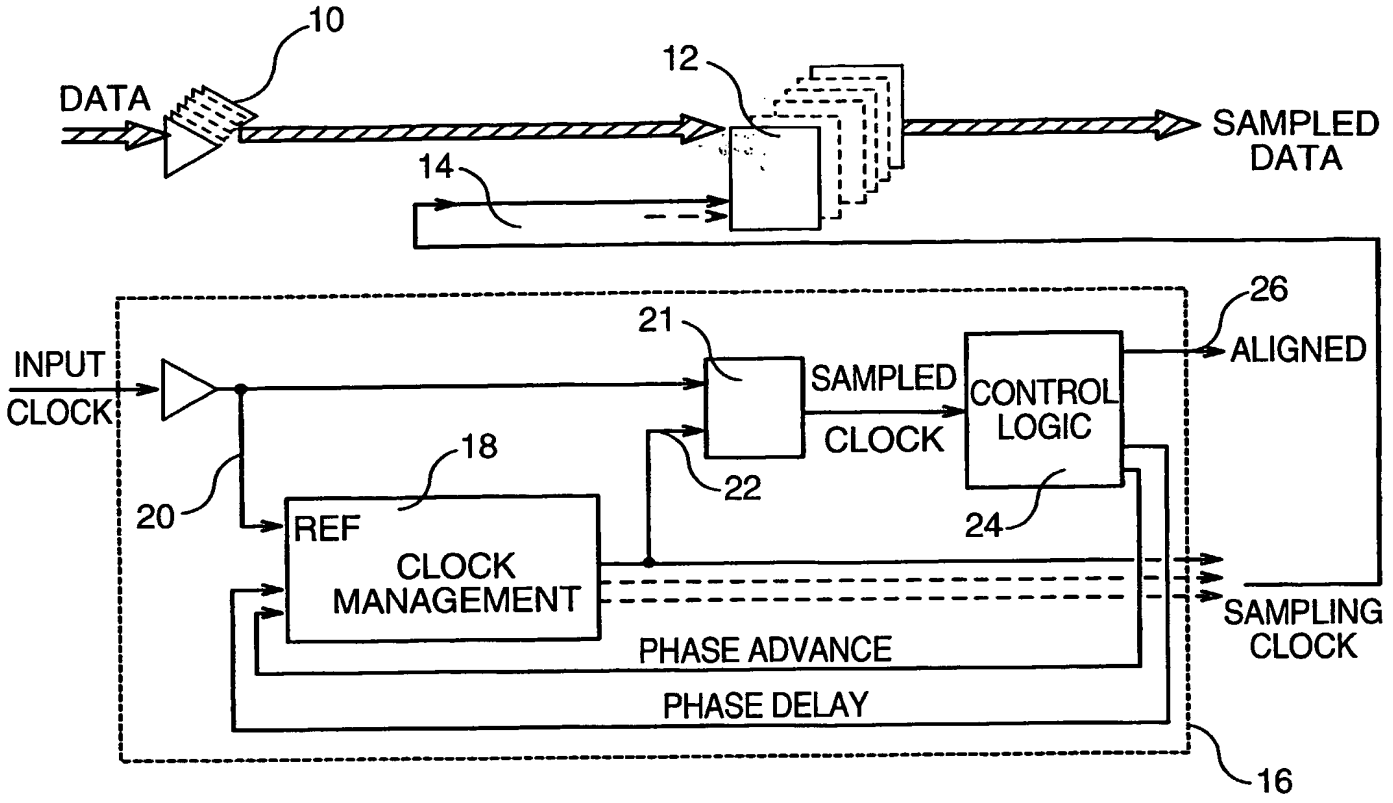
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DATA
12
SAMPLED
DATA
14
26
ALIGNED
21
INPUT
CLOCK
SAMPLED
CLOCK
CONTROL
LOGIC
18
20
22
24
REF
CLOCK
MANAGEMENT
SAMPLING
CLOCK
PHASE ADVANCE
PHASE DELAY
16

FIG. 1

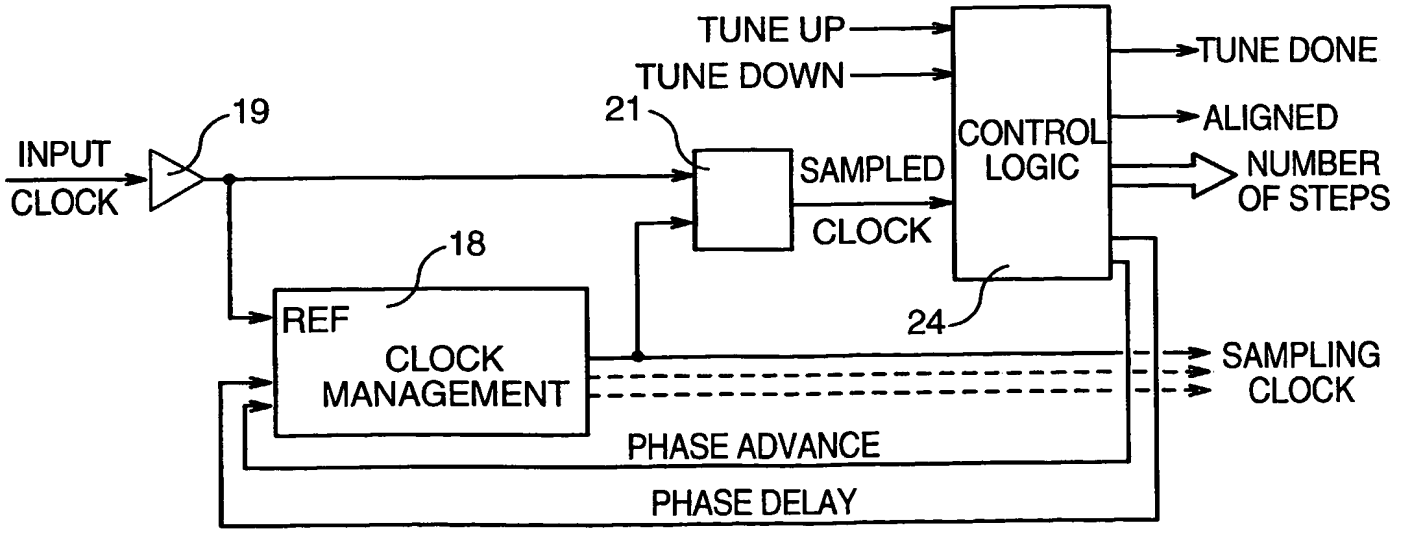
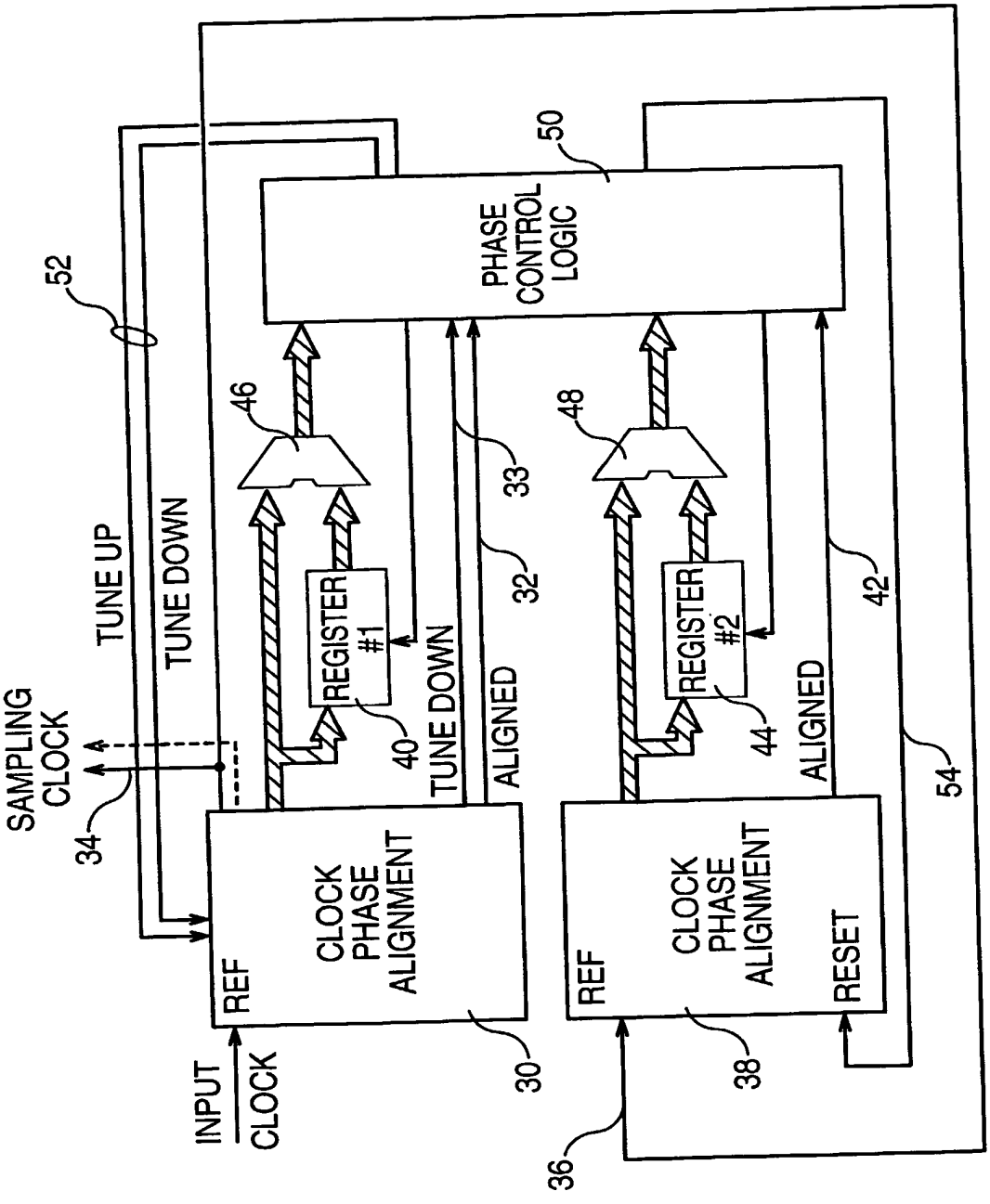

TUNE UP
TUNE DOWN
TUNE DONE
19
21
ALIGNED
INPUT
CLOCK
CONTROL
LOGIC
SAMPLED
CLOCK
NUMBER
OF STEPS
18
24
REF
CLOCK
MANAGEMENT
SAMPLING
CLOCK
PHASE ADVANCE
PHASE DELAY

FIG. 2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52
TUNE UP
TUNE DOWN
SAMPLING CLOCK
34
46
48
REGISTER #1
REGISTER #2
40
44
TUNE DOWN
ALIGNED
32
33
42
ALIGNED
54
REF
CLOCK PHASE ALIGNMENT
RESET
INPUT CLOCK
30
38
36

FIG. 3

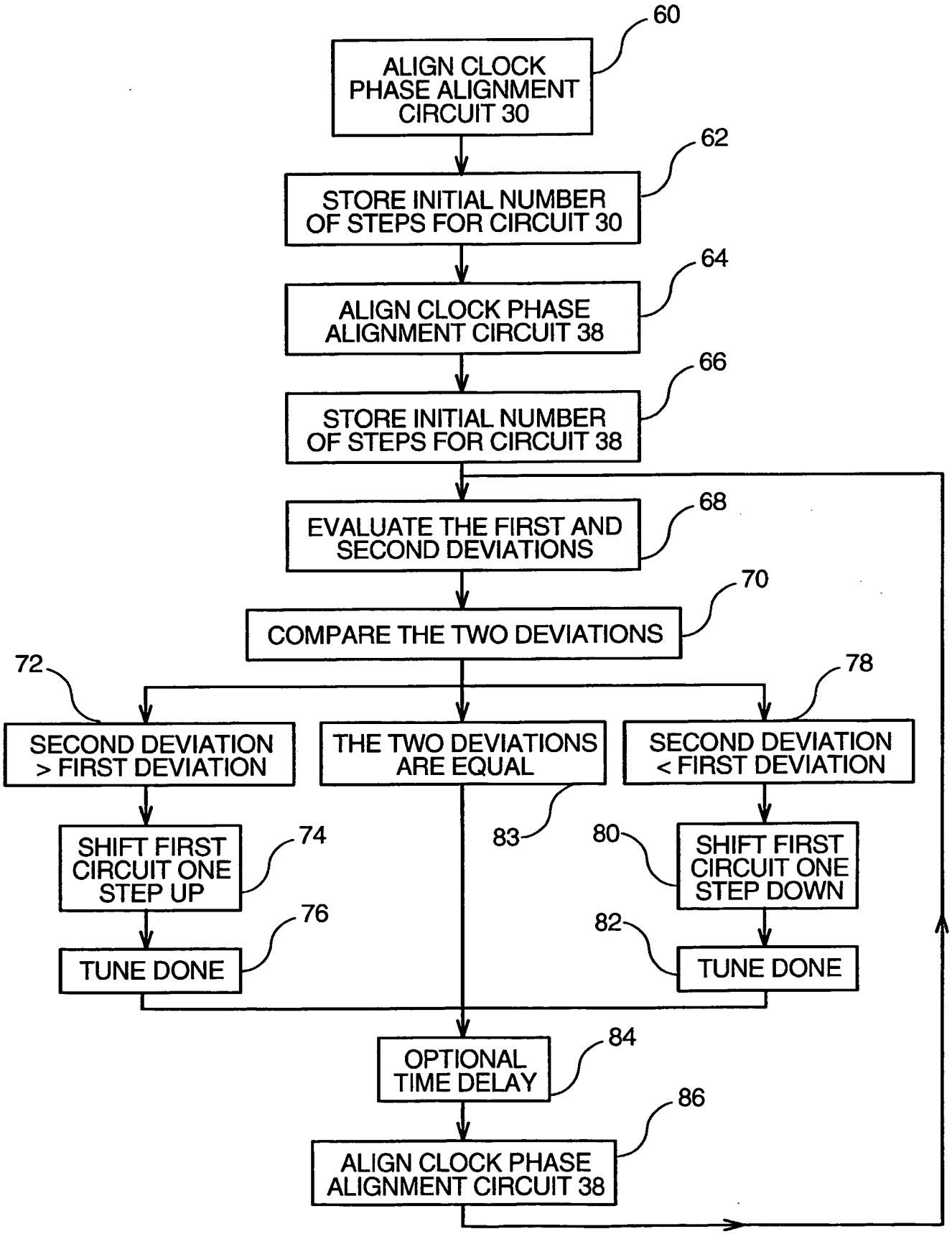
60
ALIGN CLOCK PHASE ALIGNMENT CIRCUIT 30
62
STORE INITIAL NUMBER OF STEPS FOR CIRCUIT 30
64
ALIGN CLOCK PHASE ALIGNMENT CIRCUIT 38
66
STORE INITIAL NUMBER OF STEPS FOR CIRCUIT 38
68
EVALUATE THE FIRST AND SECOND DEVIATIONS
70
COMPARE THE TWO DEVIATIONS
72
SECOND DEVIATION > FIRST DEVIATION
THE TWO DEVIATIONS ARE EQUAL
78
SECOND DEVIATION < FIRST DEVIATION
74
SHIFT FIRST CIRCUIT ONE STEP UP
76
TUNE DONE
83
80
SHIFT FIRST CIRCUIT ONE STEP DOWN
82
TUNE DONE
84
OPTIONAL TIME DELAY
86
ALIGN CLOCK PHASE ALIGNMENT CIRCUIT 38

FIG. 4

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